THAT WHICH IS CLAIMED IS:

1. An integrated search engine device, comprising:

a content addressable memory (CAM) core that is configured to support at least one database of searchable entries therein; and

a control circuit that is configured to support reporting to a command host of data that identifies entries that have been aged out of the at least one database and/or entries that have exceeded an activity-based aging threshold.

2. The device of Claim 1, wherein said control circuit is further configured to support reporting that is programmable on a per entry basis within the at least one database.

3. The device of Claim 2, wherein said control circuit comprises a first memory device that is configured to store a plurality of age report enable bits that map to respective entries in the at least one database.

4. The device of Claim 3, wherein said control circuit comprises a second memory device that is configured to store a plurality of age FIFO select bits that map to respective entries in the at least one database.

5. The device of Claim 1, wherein said control circuit is further configured to support reporting that is programmable on a per database basis.

6. The device of Claim 2, wherein said control circuit is further configured to support reporting that is programmable on a per database basis.

7. An integrated search engine device, comprising:

a content addressable memory (CAM) core that is configured to support at least one database of searchable entries therein;

at least one FIFO memory device that is configured to store addresses of entries that have been aged out of the at least one database and/or entries that have exceeded an activity-based aging threshold; and

a control circuit that is configured to support reporting of addresses from said at least one FIFO memory device to an interface of the search engine device.

8. The device of Claim 7, wherein said control circuit comprises a first memory device that is configured to store a plurality of age report enable bits that map to respective entries in the at least one database.

9. A depth-cascadable search engine device, comprising:

a content addressable memory (CAM) core that is configured to support at least one database of searchable entries therein; and

a control circuit that is configured to support reporting to a command host of addresses of first entries that have been aged out of the at least one database and addresses of second entries that have been reported as aged out to a cascade interface of the search engine device.

10. The device of Claim 9, wherein said control circuit comprises an age FIFO that is configured to store the addresses of the first and second entries pending an instance of reporting to the command host.

11. The device of Claim 10, wherein said control circuit comprises a memory device that is configured to store a plurality of age report enable bits that map to respective entries in the at least one database.

12. The device of Claim 9, wherein said control circuit comprises a memory device that is configured to store a plurality of age report enable bits that map to respective entries in the at least one database.

13. The device of Claim 10, wherein said control circuit further comprises:

a level count register that is configured to maintain a count of aged out addresses in said age FIFO; and

a level configuration register that is configured to maintain a threshold count value that specifies how many addresses of aged out entries can be stored in said age FIFO before said control circuit issues an interrupt to the command host.

14. An integrated search engine device, comprising:

a content addressable memory (CAM) core that is configured to support at least one database of searchable entries therein; and

a control circuit that is configured to support generation of at least one interrupt to a command host in response to detecting a sufficiently full storage device containing addresses of entries that have been aged out of the at least one database and/or addresses of entries that have exceeded an activity-based aging threshold.

15. The device of Claim 14, wherein said control circuit is further configured to support reporting of the addresses of the entries from the storage device to the command host, said reporting being programmable on a per entry basis.

16. The device of Claim 14, wherein the storage device comprises a FIFO memory device.

17. The device of Claim 10, wherein said control circuit further comprises:

a level count register that is configured to maintain a count of unreported addresses in said FIFO memory device; and

a level configuration register that is configured to maintain a threshold count value that specifies how many unreported addresses can be stored in said FIFO memory device before said control circuit issues the at least one interrupt.

18. An integrated search machine, comprising:

a plurality of network search engine devices that are configured in a depth-cascaded arrangement and support reporting to a command host of data that identifies entries that have been aged out of the plurality of network search engine devices and/or identifies entries that have exceeded an activity-based aging threshold.

19. The search machine of Claim 18, wherein the depth-cascaded arrangement of the plurality of network search engine devices includes a master network search engine device and at least one slave search engine device that is coupled to a cascade interface of the master network search engine device.

20. The search machine of Claim 19, wherein the data that identifies entries that have been aged out of the at least one slave search engine device is reported by the master network search engine device to the command host.